



Advanced Printed Circuit Boards and Substrates Industry Day



April 10, 2024

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Department of Defense OFFICE OF PREPUBLICATION AND SECURITY REVIEW

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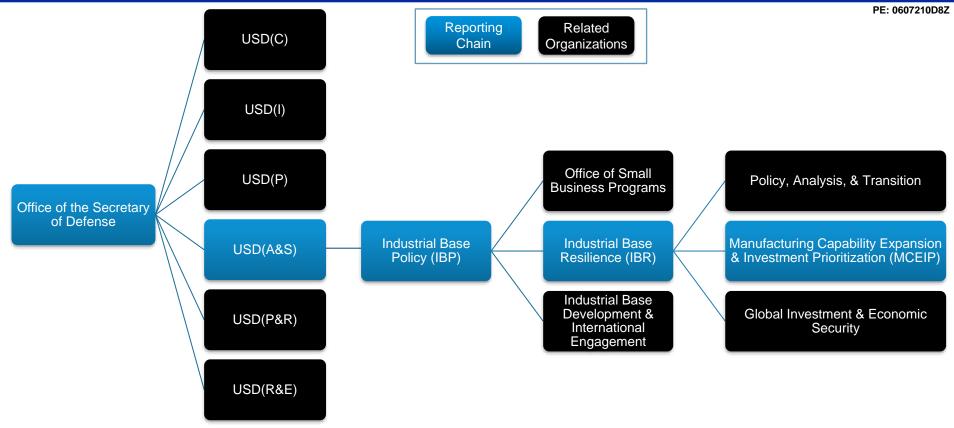


- I. Program Overview
- II. DIBC Contracting Overview
- III. Technical Element Deep Dive
 - MIC-24-001: domestic complex printed circuit board (High Density Interconnect [HDI] and/or organic Integrated
 Circuit (IC) substrate) construction and production capability and capacity;
 - MIC-24-002: domestic sourcing for enabling manufacturing materials;
 - MIC-24-003: improved microvia reliability; and
 - MIC-24-004: high-density interconnect reliability data.
- IV. Q&A Session (zoom & live)



In the DoD Ecosystem



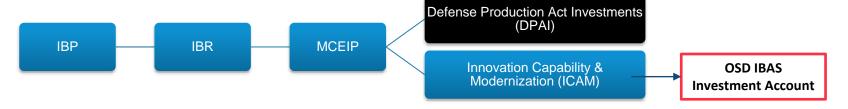




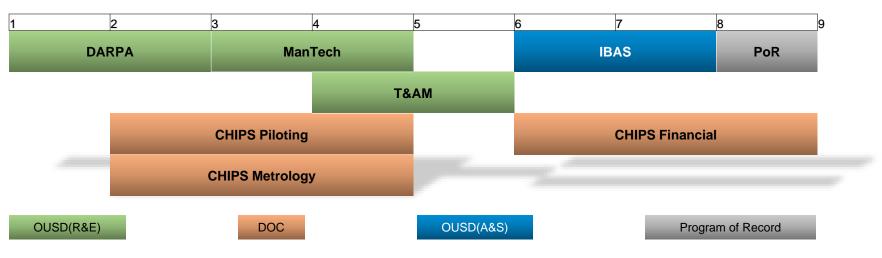
In the USG Ecosystem







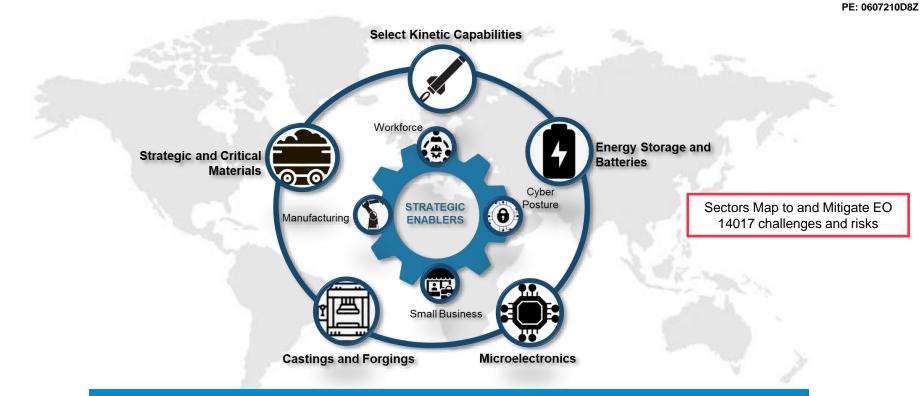
Technology Readiness Levels (TRLs)





In the IBAS Program: Sectors





Help IBP **build supply chain reliability and resiliency** through workforce development and other industrial capacity initiatives



In the IBAS Program: Goals

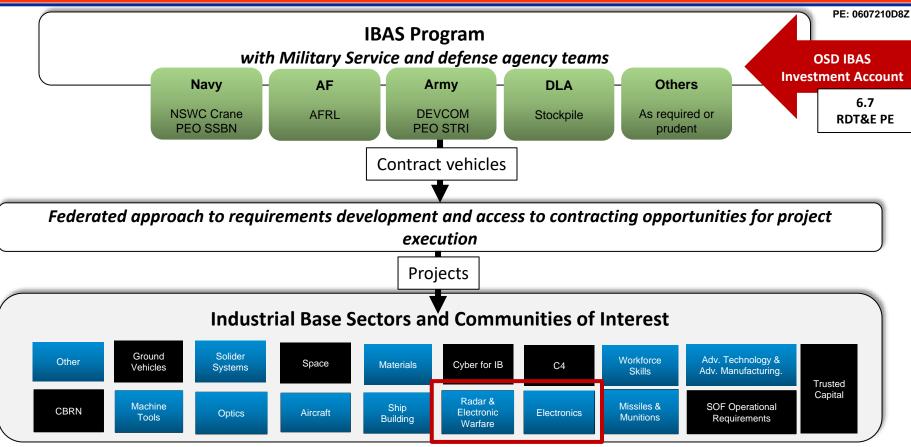


PE: 0607210D8Z





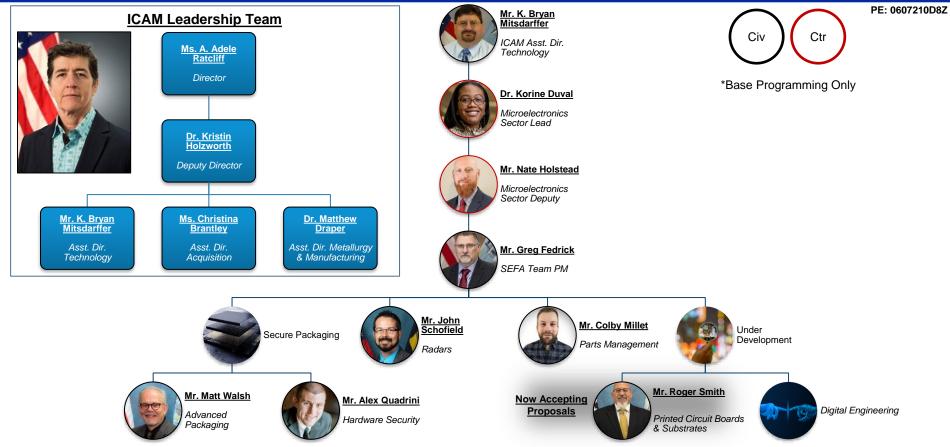
In the IBAS Program: "Federated" Approach





In the Sector: Overview*



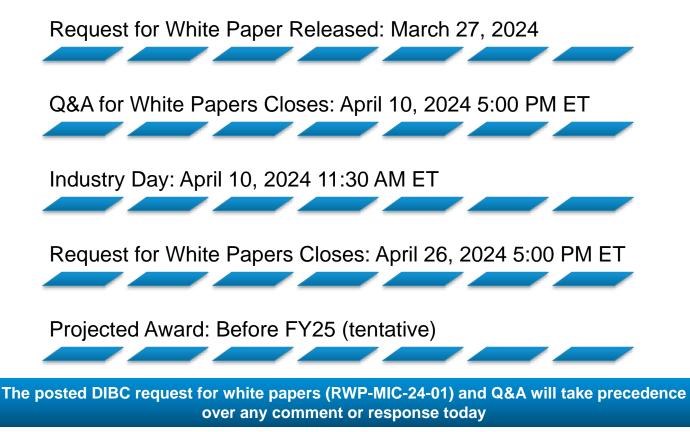




Request for White (RWP) Papers Overview



PE: 0607210D8Z





Technical Topic Areas



PE: 0607210D8Z



TE1: Printed circuit board construction, production capability, and capacity

≤75 µm microvias
≤50 µm traces and spaces
≤50 dielectric thickness

TE2: Enabling materials for manufacturing

•Advanced electronic materials for DoD applications



TE3: Improved microvia reliability

- Applications in HDI, UHDI, organic IC substratesDesign rules
- •Process parameters



TE4: HDI and/or Organic IC Substrate reliability data

•Standards for reliability •Test methods for reliability



Program Goals













Contact us at:

https://www.dibconsortium.org/contact-us/

osd.pentagon.ousd-a-s.mbx.ibas@mail.mil

https://www.businessdefense.gov/ibr/mceip/index.html



Defense Industrial Base Consortium (DIBC) OTA & Contracting Overview

10 April 2024





 OTA Overview
 DIBC Specifics
 RWP-MIC-24-01: Advanced Printed Circuit Boards and Electronic Substrates



OTA Overview

3

What is an OTA?



Other Transaction Agreements (OTA) are legally binding agreements that can be used to carry out research projects that meet the stipulations that are set forth in two sections of law:

• 10 U.S. Code 2371

grants the authority to use other transactions to carry out **basic**, **applied**, **and advanced research projects**.

• 10 U.S. Code 2371b

permits the use of other transactions to conduct **prototype projects and follow-on production**.

OTA collaborations give government **a single entry point** to hundreds of organizations, including nontraditionals. Competitions are held for every project awarded through an OTA-based collaboration.

OTA Requirements



Each award must meet one of the following:

- at least one non-traditional defense contractor or nonprofit research institution participating to a significant extent in the prototype project, or
- all significant participants in the transaction other than the Federal Government are small businesses or nontraditional defense contractors, or
- at least one third of the total cost of the prototype project is paid out of funds provided by sources other than the Federal Government.

Non-Traditional Defense Contractor

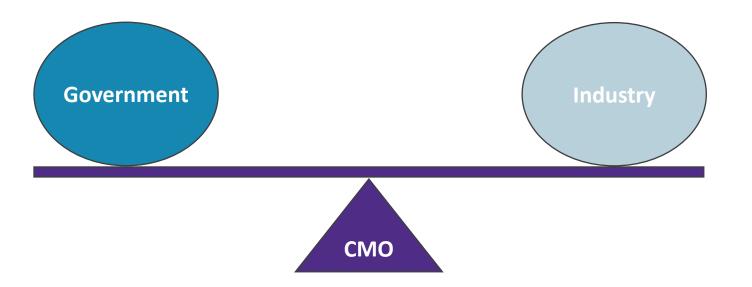


- Non-traditional Defense Contractor
 - A nontraditional defense contractor means an entity that is not currently
 performing and has not performed, for at least the one-year period preceding the
 issue date of a Spectrum Request for Prototype Proposal, any contract or
 subcontract for the Department of Defense that is subject to full coverage under
 the cost accounting standards prescribed pursuant to section 1502 of title 41 and
 the regulations implementing such section.
- "Significant Extent" or "Significant Contribution" by a Non-traditional Defense Contractor could include:
 - Supplying new key technology or products
 - Accomplishing a significant amount of the effort
 - Causing a material reduction in the cost or schedule, or increase in performance

ATI's CMO Role



ATI, as the "Consortium Management Organization (CMO)", serves as the critical pivot point between Government and Industry.



ATI ensures the needs of both are balanced and met in an efficient and expeditious manner.

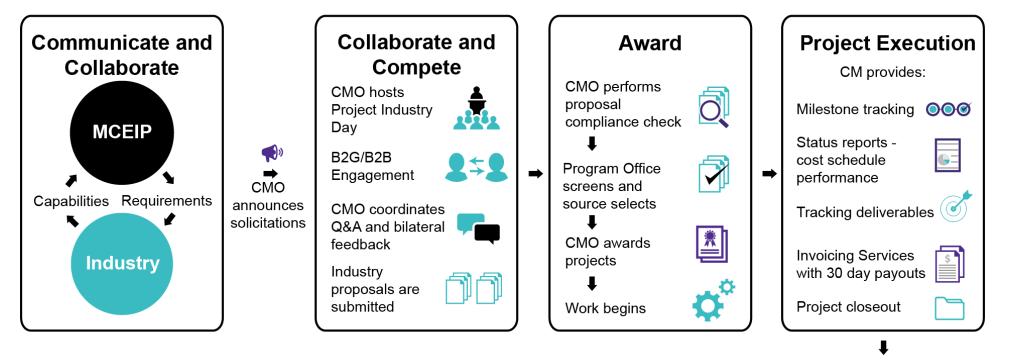
The Consortium Model Benefits Both Government + Industry Stakeholders and Prioritizes Innovation

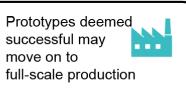


EFENSE INDUSTRIA BASE CONSORTIUM

Problem Statements to Successful Outcomes









DIBC Specifics

10

DIBC Mission/Vision

• Mission:



 To coalesce and expand the Defense Industrial Base (DIB) in support of the Manufacturing Capability Expansion & Investment Prioritization (MCEIP) critical subsectors. MCEIP is focused on addressing defense supply chain issues, developing the industrial workforce, sustaining critical production, commercializing R&D efforts, and rapidly scaling emerging technologies to build a robust, resilient DIB.

• Vision:

• To deliver a resilient U.S. supply chain and workforce able to respond in times of national security crisis without reliance on foreign sources.

• Critical sectors

- Kinetic Capabilities (Hypersonics), Energy Storage and Batteries, Microelectronics, Castings and Forgings, Strategic and critical materials, Workforce development
- Additional areas of interest
 - Small Unmanned Aerial Systems (sUAS), Biomanufacturing, Space Industrial Base, Submarine Industrial Base

Project Pathway Plan

- One Step: Full Cost & Technical Proposal
- Two Step: Enhanced White Paper (up to 15 pages)
 - White Paper
 - If selected, full cost proposal
- Three Step Approach
 - White Paper
 - After evaluations, selectees invited to Pitch
 - If selected after Pitch, full cost proposal



Two Step Process Overview: Enhanced Whitepapers



BIDS Overview



This BIDS Portal is a customizable tool used to manage the collection of requirements, proposal or white paper submission, technical evaluations, and feedback release.

DEFENSE INC	Welcome, Joshua Doyle FAQs Help Request USTRUE Portal DIBC Home To Do List Submissions Reports Dashboard Search Logout	
Admin Tools RPP/RWP Configuration Dashboard Evaluator Tools To Do List My Evaluations	RPP/RWPs - Open On January 25, 2024, the RPP/RWP (DIBC-24-TEST4-1-25 (Chris Test 4)) was released. Enhanced Whitepapers are due by January 29, 2024 at 02:00:00 PM ET. Please note, in accordance with the DIBC Request for Prototype Projects (RPP), all responses must be received by the response date on the first page of the RPP/RWP or RPI (unless modified in an amendment). Neither the Government nor ATI can make allowances/exceptions for submission problems encountered by the offeror using system-to-system interfaces with BIDS. If the offeror receives errors and fails to upload the full submission prior to the submission will not be accepted. All information related to this solicitation is located on the Members Only portion of the DIBC website:	Need Help? FAQs Answers some general questions. See DIBC Members Only site for detailed FAQ.
RPP/RWP Requirements My Requirements Funding Table Submissions	Defense Industrial Base Consortium The DIBC Other Transaction Agreement (OTA) will accelerate Department of Defense (DoD) access to technologies typically reserved for commercial development. The consortium managed OT Agreement will enhance MCEIP's mission of addressing defense supply chain issues, developing the industrial workforce, sustaining critical production, commercializing Research and Development (R&D) efforts, and rapidly scaling emerging technologies to build a robust, resilient DIB.	Help Request Request help about this website. Contact Help Request website help.
Search RPP/RWP Archives RPP/RWP Responses Competitive Evaluations	DIBC Membership Note: In order to receive an award in response to any solicitation on this site, you must be a member of the Defense Industrial Base Consortium. For more information on becoming a member, please visit: https://www.dibconsortium.org/how-to-join/	Contact DIBC Request proposal help. Reference Materials Download reference
Reports Spreadsheet Reports Account Center Edit My Account Change Password Logout	SECURITY NOTICE: Unauthorized attempts to deny service, upload information, change information, or attempt to access a non-public site from this service are strictly prohibited and may be punishable under Title 18 of the U.S. Code to include the Computer Fraud and Abuse Act of 1986 and the National Information	materials, such as quick cards and training materials.
nformation	CLOS Convicted © 2024 All Dickle Dessand This workide was scatted by the Associates and is and of the BIDS family	

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RWP-MIC-24-01

RWP Guidelines

DEFENSE INDUSTRIAL BASE CONSORTIUM

- Read the RWP, read it again, and read it again
 - Follow submission format and utilize the EWP template
- Create a BIDS account early and review the submission site prior to the due date
- Don't be afraid to ask questions:
 - All questions should go to: <u>DIBC.Contracts@ati.org</u>
- Submit white papers prior to the deadline
- Must be a DIBC member to receive an award....apply now

After You Submit



- Be prepared to provide any requested revisions that are found during compliance screening
 - Conducted one day after due date
- Government will perform technical evaluations
 - Includes Met or Not Met ratings
 - May include award recommendations as well
- Feedback released in BIDS
- If selected for award, will be asked to provide SOW and cost proposal, along with several other forms
- Upon government direction, ATI will issue the award to the DIBC member once government and awardee finalize SOW, and costs analysis is complete





Advanced Printed Circuit Boards and Substrates Industry Day



April 10, 2024 Innovation Capability and Modernization Office (ICAM) Technical Element Deep Dive





Technical Element 1 Ultra High Density Interconnects (UHDI) Organic Integrated Circuit (IC) Substrates

Kathy Nargi-Toth, ctr







Domestic complex printed circuit board construction and production capability and capacity MIC-24-001:

Prototype the development of domestic sources for printed board and/or organic IC substrates that have approximately ≤75 µm microvias, ≤50 µm traces and spaces, and ≤50 µm dielectric thickness and expand domestic capability and capacity to produce such products. This can include investments in prototyping various semi-additive process capabilities and capacity, building on those delivered by traditional subtractive processes.





- Reliable medium volume 25-65 µm lines/spaces
- High reliability in \geq 3 layers of stacked microvias
- BGA pitch ≤ 0.3 mm
- High frequency applications (50 Ghz and above)
- Industrial standards for high reliability applications of UHDI products (design and performance)
- Reliability data to support new designs and materials



U.S. State of the Practice



PE: 0607210D8Z

- Manufacturing norm: 75 µm lines and spaces
- Limited capability: ~ 60 µm lines and space
- Predominantly subtractive manufacturing
- Limited stacked microvia capability for high reliability applications
- Developmental UHDI capabilities
- Developmental organic IC substrate capabilities



Products Beyond IPC 226 Criteria



PE: 0607210D8Z

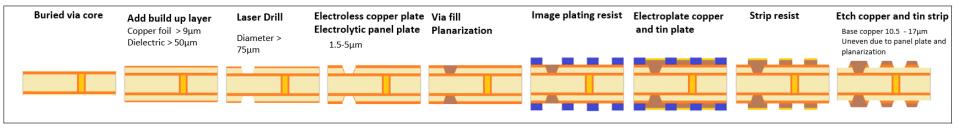
		Level C	50-40 um	40-30 um	30-20um	< 20 um
IPC-2226 HDI Type ref.	Features	<u>I,II,III,IV, V, VI</u>				
b	Microvia diameter at capture land (as formed, no plating)	75 µm [0.003 in]	50um - 75um	<25um	35um - 75um	35um - 75um
S	Print & Etch conductor trace width	50 µm [0.002 in]	40um - 50um	N/A (additive)	N/A	N/A
t	Print & Etch conductor spacing	50 µm [0.002 in]	40um - 50um	N/A (additive)	N/A	N/A
E5	Plated conductor trace width	50 µm [0.002 in]	40um - 50um	30um – 40um	20um - 30um	6um - 20um
F5	Plated conductor spacing	60 µm [0.0024 in]	40um - 50um	30um - 40um	20um - 30um	6um - 20um
h	Through via diameter (as formed, prior to plating)	See Table 5-2	150 um (restricted)	N/A	N/A	N/A
i	Minimum through via hole wall plating thickness	See IPC-2221, Table 4-3	<20um (TBA)	N/A	N/A	N/A
j	Dielectric thickness (HDI blind microvia layer)(2)	< 50 µm [0.002 in]	25um - 50um	10um - 40m	10um - 40um	3um - 25um
k	Cu foil thickness to be Plated (This represents the maximum foil thickness to achieve features "e" and "f" for one plating step)	1⁄8 oz. (See IPC-2221, Table 10-2)	3um - 8.5um	1-5 um	> 1 um	none – 1 um
k'	Cu foil thickness for Print & Etch (This represents the maximum foil thickness to achieve features "s" and "t")	1⁄4 oz. (See IPC-2221, Table 10-1)	3um - 17.1um	None	none - 8.5um	none - 8.5um
m	Minimum blind microvia hole plating thickness	12 µm [0.0047 in]	Filled	Filled	Filled	Filled
m'	Minimum buried microvia hole plating thickness	12 µm [0.0047 in]	Filled	Filled	Filled	Filled
n	Minimum buried via hole wall plating thickness	See IPC-2221, Table 4-3	12um - 20um	N/A	12um - 20um	12um - 20um
0	Buried via diameter (as formed, no plating)	See IPC-2221, Table 9-4	150 um	N/A		

Excerpt from the IPC-D-33 AP Working Draft



Subtractive Process vs mSAP Process

PE: 0607210D8Z



Conventional subtractive etch Line width and spacing >50 microns (typical in U.S. is 75 microns)

mSAP (modified semi-additive) Line width and spacing >20µm

Buried via core	Add buildup layer Copper foil 1.5 - 3 micron Dielectric < 50 microns	Laser Drill Diameter < 75μm	Electroless copper plate .75 - 1.5µm	Image plating resist	Electroplate copper	Strip resist	Differential etch – no etch resist Mild micro-etch type final etchant Base copper 2.25 – 4.5µm Very uniform thickness	
		Requires latest generation laser drilling equipment capable of 30 – 50µm diameters	Specialized electroless copper with thinner finer deposit	Requires direct imaging equipment capable of 20µm lines and spaces and specialized high resolution resist	Uses specialized plating equipment and chemistry to fill vias and plate conductor simultaneously		Etching equipment, chemistry is designed specifically for mSAP. Etchant is anisotropic with low etch rate compared to conventional etchants	AOI equipment requires 20µm resolution Requires low etch rate oxide coating





- Clean rooms / minimizing particulates in air, chemistry, equipment
- Automated material handling throughout manufacturing
 - Conveyorized developers, strippers, oxide, thin material handling
- Laser drill < 50 µm diameter capability
- Direct imaging <= 20 µm line and space capability
- AOI capability <= 20 µm line and space capability
- Electrical test <= 0.3 mm pitch capability
- Specialized via fill plating equipment
- Advanced materials
 - Thin copper foils, advanced laminates, build-up films, thin electroless copper, highresolution photoresists, via fill chemistry, low etch rate oxide and etching, highresolution solder masks
- Semi-additive processes (SAP) and modified SAP (mSAP)



Technical Element 1 Conclusion



- UHDI printed boards are needed to meet the requirements of next-generation DoD products
- The U.S. printed board manufacturing base has limited capability and capacity to produce UHDI products and organic IC substrates
- There are differences in facility, equipment, material and process requirements between conventional HDI and UHDI, with additional changes needed to move from UHDI to organic IC substrates
- Standards, testing, and qualification criteria to meet DoD reliability requirements are needed for UHDI products





Technical Element 2 Domestic Sourcing for Enabling Materials for Manufacturing

Tina Landon



Technical Element 2



PE: 0607210D8Z

Domestic sourcing for enabling materials for manufacturing (MIC-24-002):

Prototype state-of-the-art capabilities to enable the development of advanced materials for DoD applications (e.g., copper foils for modified semi-additive applications, build-up film equivalents, advanced laminates for organic IC substrates, and solder masks for organic IC Substrate applications).





- Global growth in the microelectronics industry has produced an asymmetric and interdependent relationship between Asia's critical role in production and regions such as the U.S. which control key inputs into the value chain.
 - Intellectual property (IP) for microelectronics design is concentrated in the U.S. and allied nations; production, assembly and testing happens in Asia. Geopolitical considerations produce uncertainty about future evolution in this value chain.
 - Technological sovereignty requires economic decoupling of the electronics industry in the U.S. from overseas activities, which may disrupt U.S. plans and production.



Overview / Need



PE: 0607210D8Z

- Essential materials must be obtained from overseas suppliers
 - Materials (e.g., build-up films for advanced board construction)
 - Domestic equipment capability (e.g., photolithography equipment)
- Human capital risks developing as dependence on overseas supply increases; lack of domestic skill threatens growth
- Geographical, political, and environmental threats jeopardize continuity and predictability for microelectronics access

Causes of Instability:

- Pandemic
- Infrastructure
 - Fire at Japanese chipmaker Renesas Electronics
 - Winter weather in Texas cutting power to Samsung facility
 - 2024 earthquake halting production at Toshiba
- Global shortfalls in shipping capacity



Reshoring and Maintaining



PE: 0607210D8Z

- Indigenizing the entire supply chain for advanced electronics is challenging and expensive. Together, the U.S. and its allies* enjoy a competitive advantage at nearly every step of the supply chain.
- "Protect" and "promote" policies aimed at improving supply chain security are desirable to maintain leadership in the microelectronics industry
 - Leadership in development of circuits that enable use of state-of-the-art logic chips, which perform power advanced applications like artificial intelligence
 - Improved access to circuit card fabrication techniques for UHDI
- By controlling production of advanced electronics, the U.S. and allied democracies ensure these technologies are developed and deployed safely and ethically to broadly benefit the world

*Key stakeholders including Japan, the Netherlands, Taiwan, South Korea, the United Kingdom, and Germany



Essential Materials



- Copper foil for printed circuits
 - One U.S. producer produces mainstream (standard) product
 - Other industry leaders source foils from offshore sources, including advanced foils for high speed / low loss and mSAP applications
- Supply chain for glass fiber and woven e-glass products includes sources in Japan, Taiwan, China
 - China is a major producer (53%) and consumer of e-glass; U.S. has 4+ domestic manufacturers for basic glass fiber
 - Advanced glass capabilities limited to Japan and Taiwan suppliers (flat glass, low Dk glass, silica-based fillers)



Essential Materials



PE: 0607210D8Z

- Organic resins
 - Well-developed Asian supply chain
 - Resin manufacturing often co-located with filler and advanced silica particle manufacturing (Japan)
 - Some U.S. specialty chemical suppliers
 - Need to have access to complete supply chain, including advanced reinforcement, located in U.S.
- Substrates
 - Build-up films, high-performance solder masks primarily sourced from Japan
 - EPA reviews and Toxic Substances Control Act registry required for imported material

Principal Printed Board Resins

- Ероху
- Phenolic
- Polyimide
- Polytetrafluoroethylene (PTFE)
- Bismaleimide-triazine (BT)
- Cyanate ester
- Polyphenylene ether (PPE)
- Liquid crystal polymer (LCP)





- Per- and polyfluoroalkyl substances (PFAS) chemicals
 - PFAS (such as PTFE) are an integral part of chemical manufacturing operations for semiconductors, substrates, and printed boards; limited alternatives available
- Lead-free solder
 - China is the leading producer of refined tin
 - 97% of tin comes from developing nations with 40% from small-scale mining
 - Tin reserves are declining, with deficits anticipated by 2030
- Solder masks
 - State-of-the-art dry film material available domestically; some liquid photoimagable (LPI) not available at this time.
 - R&D exemption required for import of some products





Technical Element 3 Improved Microvia Reliability

Matthew McQueen



Technical Element 3



PE: 0607210D8Z

Improved microvia reliability (MIC-24-003):

Prototype new models for improving microvia reliability across various manufacturing sources. Develop and validate design rules and process parameters that yield stable / reliable results on current and emerging HDI, UHDI, and/or organic IC substrate technologies. This could involve a detailed design of experiments (DOE) involving printed board designers, manufacturers, process equipment, chemistry, and materials suppliers.





- The DoD requires state of the industry, ideally state of the art, electronics to maintain and extend technical advantage
- Many DoD programs adopt technologies as a function of the risk that would be accepted and the impact of the potential failure
- The inability of much of the domestic printed circuit supply base to provide consistent, robust, and reliable microvia products has caused extended critical program timelines and early life electrical failures

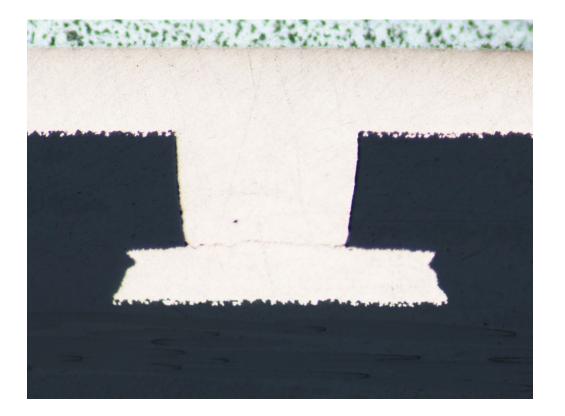


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Critical Issue



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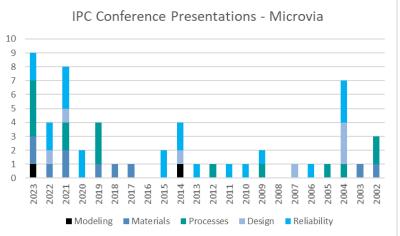




Recent Industry Efforts



- IPC Weak Interface Microvia Failures Technology Solutions Subcommittee (IPC-V-TSL-MVIA)
 - Initiated after IPC White Paper "Via Chain Continuity Reflow Test: The Hidden Reliability Threat – Weak Microvia Interface" in 2018 (IPC-WP-023)
 - Efforts have stalled due to inactivity and funding concerns
- HDP User Group
 - "PCB Feature Miniaturization"
 (HDP202307R) released May 2023





Military Printed Board Evaluation Methods



PE: 0607210D8Z

Origination of current military specification (MIL-SPEC) requirements for rigid multilayer boards:

• Thermal Stress (Solder Float)

- IPC-TM-650 2.6.8 (MIL-P-55110 initial release 1960)

- Thermal Shock (-65° C / 125° C)
 - IPC-TM-650 2.6.7A (Released August 1997)
- DC Current Induced Temperature Cycling
 - IPC-TM-650 2.6.26 (Released May 2001 [IST])
 - Revised to add current induced thermal cycling (June 2014)
- Thermal Stress Convection Air Reflow
 - IPC-TM-650 2.6.27 (Released May 2009)





- Create strong correlations between models or simulations, test data, and real product failure modes
- Challenge and/or revalidate design and manufacturing assumptions that may need to be updated
- Document methods and best practices to grow and improve the domestic printed board industrial base capability to produce reliable microvia products





Technical Element 4 HDI/UHDI Reliability Data

Daniel McCormick



Technical Element 4



PE: 0607210D8Z

HDI and/or organic IC substrate reliability data (MIC-24-004):

Develop and prototype standards and test methods which assess the reliability characteristics of design rules, materials, and processes for HDI, UHDI and/or organic IC Substrate features. Other prototyping and test efforts could include sponsored and comprehensive highly accelerated stress testing of HDI and UHDI structures to assess long term operational reliability in high stress environments. Test requirements should be incorporated into relevant industry and DoD requirements and documents.



Overview/Need



- HDI/UHDI Reliability Data Needs
 - Develop and prototype standards and test methods assessing:
 - Design rules, materials, and processes for HDI/UHDI technologies
 - Sponsor comprehensive highly accelerated stress testing of HDI/UHDI structures to access:
 - Long term operational reliability in high stress environments
 - Incorporate test requirements into relevant industry and DoD requirements documents
 - Obtain HDI/UHDI reliability data supporting technologies applied to high reliability applications, e.g., automotive, aerospace, DoD, and medical



State of the Industry



- HDI/UHDI Reliability Data Status
 - Concerted effort to develop IPC UHDI industry standards for high reliability products
 - Reliability data must support UHDI validation and verification to include:
 - UHDI base design technologies, materials, and processes
 - UHDI board and systems level design and applications implementation
 - UHDI quality and reliability test and analysis methods and applications
 - Develop HDI/UHDI reliability data utilizing commonly accepted data types to support design, analysis, and test

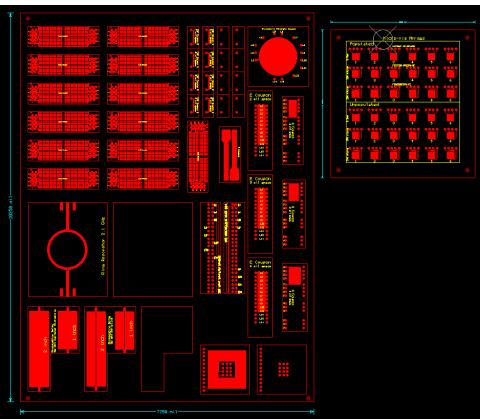


PrCB EA-Designed UHDI Test Vehicle



PE: 0607210D8Z

- 14 layer 6-2-6 sequentially laminated high-density build-up stack-up
- 1-6 microvia layers
- Stacked verses staggered
- Four microvia diameters: 0.001" 0.002" 0.003" 0.004"
- Three microvia array pitches
- Two laminate CTEs
- Available for use!



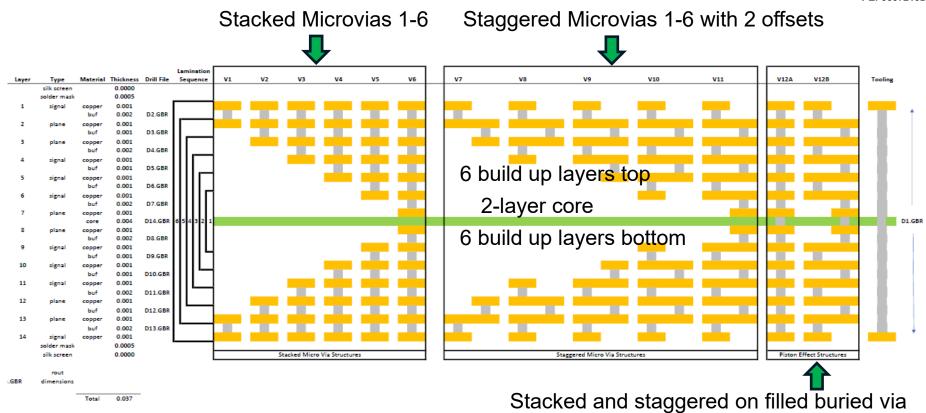


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UHDI Test Vehicle – Stack-Up









Acronyms



- BT bismaleimide-triazine
- DoD Department of Defense
- DOE design of experiments
- EPA Environmental Protection Agency
- HDI high density interconnect
- IC integrated circuit
- IP intellectual property
- LCP liquid crystal polymer
- LPI liquid photoimagable

- MIL-SPEC military specification
- mSAP modified semi-additive process
- PFAS per- and polyfluoroalkyl substances (PFAS)
- PPE polyphenylene ether
- PTFE polytetrafluoroethylene
- SAP semi-additive process
- UHDI ultra high density interconnect









Contact us at:

https://www.dibconsortium.org/contact-us/

osd.pentagon.ousd-a-s.mbx.ibas@mail.mil

https://www.businessdefense.gov/ibr/mceip/index.html